ES_LPC18S5x/S3x Flash

Errata sheet LPC18S5x, LPC18S3x, flash-based devices

Rev. 1.1 — 23 October 2015 **Errata sheet**

Document information

Info	Content
Keywords	LPC18S57JET256; LPC18S57JBD208; LPC18S37JBD144; LPC18S37JET100; ARM Cortex-M3 flash-based devices errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
1.1	20151023	• Added RESET.2
1	20150213	• Initial version

Contact information

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1. Product identification

The LPC18S5x/S3x flash-based devices (hereafter referred to as 'LPC18S5x') typically have the following top-side marking:

LPC18S5xxxxxxx

xxxxxxxx

xxxYYWWxR[x]

The last/second to last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC18S5x flash-based devices:

Table 1. Device revision table

Revision identifier (R)	Revision description
'A'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
EEPROM.2	Reset values for the RWSTATE and WSTATE registers in the EEPROM block are different from what is shown in the user manual.	'A'	Section 3.1
EMC.1	Operating frequency of EMC lower than data sheet value.	'A'	Section 3.2
I2C.1	In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register.	'A'	Section 3.3
SRAM.1	SRAM in deep sleep and power down modes may lose state.	'A'	Section 3.4
USB.1	USB0 unable to communicate with low-speed USB peripheral in host mode when using full-speed hub.	'A'	Section 3.5
USB.2	The USB_SOF_Event may fire earlier than expected and/or a false interrupt may be generated.	'A'	Section 3.6
USBROM.1	Nested NAK handling of EP0 OUT endpoint.	'A'	Section 3.7
USBROM.2	Isochronous transfers.	'A'	Section 3.8
SD/MMC.1	Data CRC error returned on CMD6 command.	'A'	Section 3.9
RESET.1	Master Reset (MASTER_RST) and M3 Reset (M3_RST) are not functional.	'A'	Section 3.10
RESET.2	Loss of device functionality on reset via nRESET in deep-sleep and power-down mode.	'A'	Section 3.11

Table 3. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3. Functional problems detail

3.1 EEPROM.2

Introduction:

A 16 kB EEPROM is available on these parts which operates up to 180 MHz. Registers in the EEPROM define the number of wait states that are applied to read and write operations on the device.

Problem:

The reset values for the RWSTATE and WSTATE registers in the EEPROM block are different from what is shown in the user manual.

Table 4. Reset values for RWSTATE and WSTATE

	Reset value for Rev '-' parts	Reset value in the Users Manual
RWSTATE	0000 0905	0000 0E07
WSTATE	0002 0602	0004 0802

Work-around:

No workaround needed. Program the required values into the registers before using the EEPROM.

3.2 EMC.1

Introduction:

The LPC18Sxx parts contain an External Memory Controller (EMC) capable of interfacing to external SDRAM, SRAM, and asynchronous parallel flash memories. The EMC can be configured to operate at the processor core frequency (BASE_M3_CLOCK) or the core frequency divided by 2.

Problem:

For SDRAM, the electrical characteristic of the LQFP144 and LQFP208 packages limits the operating frequency of the EMC to a certain level, which is lower than the specified value in the data sheet. Choosing an SDRAM clock of 72MHz as the upper limit provides some safety margin. This frequency is either achieved by a core and EMC frequency of 72MHz, or by a 144MHz core and a 72MHz EMC frequency. However, SDRAM performance can vary depending on board design and layout.

Work-around:

There is no work-around.
The upper limit of the SDRAM clock frequency is highly dependent on the PCB layout and the quality of the power supply and de-coupling circuitry.

3.3 I2C.1

Introduction:

The I2C monitor allows the device to monitor the I2C traffic on the I2C bus in a non-intrusive way.

Problem:

In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I2C bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1); //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to the slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for the slave-transmitter mode:

```
case 0xA8:     // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:     // data byte in DAT transmitted, ACK received
case 0xC0:     // (last) data byte transmitted, NACK received
case 0xC8:     // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER;//Save data. Data can be process in Main loop
    LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```

3.4 SRAM.1

Introduction:

SRAM state is retained in deep sleep and power down modes.

Problem:

Incorrect settings may lead to SRAM state retention loss over time and temperature. This can cause erratic behavior due to SRAM data loss after wake-up from deep sleep mode or power down mode.

Work-around:

Reserved register at 0x4004.3008 bits 17:16 should be set to 0x2 before entering deep sleep mode or power down mode.

```
#define CREG0_008       (0x40043008)
#define PD0_SLEEP0_MODE (0x4004201c)

#define PMC_PWR_DEEP_SLEEP_MODE 0x3F00AA
#define PMC_PWR_POWER_DOWN_MODE 0x3FFCBA

unsigned int regval;

// EXAMPLE 1:
regval = *((unsigned int *) CREG0_008);
regval |= (1 << 17);
regval &= ~(1 << 16);
*((unsigned int *) CREG0_008) = regval;

// prepare for entering deep sleep
*((unsigned int *) PD0_SLEEP0_MODE)  = PMC_PWR_DEEP_SLEEP_MODE;

// enter deep sleep
__wfi();

// EXAMPLE 2:
regval = *((unsigned int *) CREG0_008);
regval |= (1 << 17);
regval &= ~(1 << 16);
*((unsigned int *) CREG0_008) = regval;

// prepare for entering power down
*((unsigned int *) PD0_SLEEP0_MODE)  = PMC_PWR_POWER_DOWN_MODE;

// enter power down
__wfi();
```

3.5 USB.1

Introduction:

The LPC18S5x parts include two USB 2.0 controllers that can operate in host mode at high-speed. One of these controllers, USB0, contains an on-chip high-speed UTMI+ compliant transceiver (PHY) which supports high-speed, full-speed, and low-speed USB-compliant peripherals.

Problem:

The USB controller called USB0 is unable to communicate with a low-speed USB peripheral in host mode when there is a full-speed hub directly connected to the USB0 port and a low-speed peripheral is connected in the tree somewhere below this full-speed hub. Only USB0 has this problem; the other USB controller, USB1 does not.

Work-around:

There is no work-around for this problem. It is suggested that the low-speed USB peripheral is either connected directly to USB0 or a high-speed hub is placed between that peripheral and USB0.

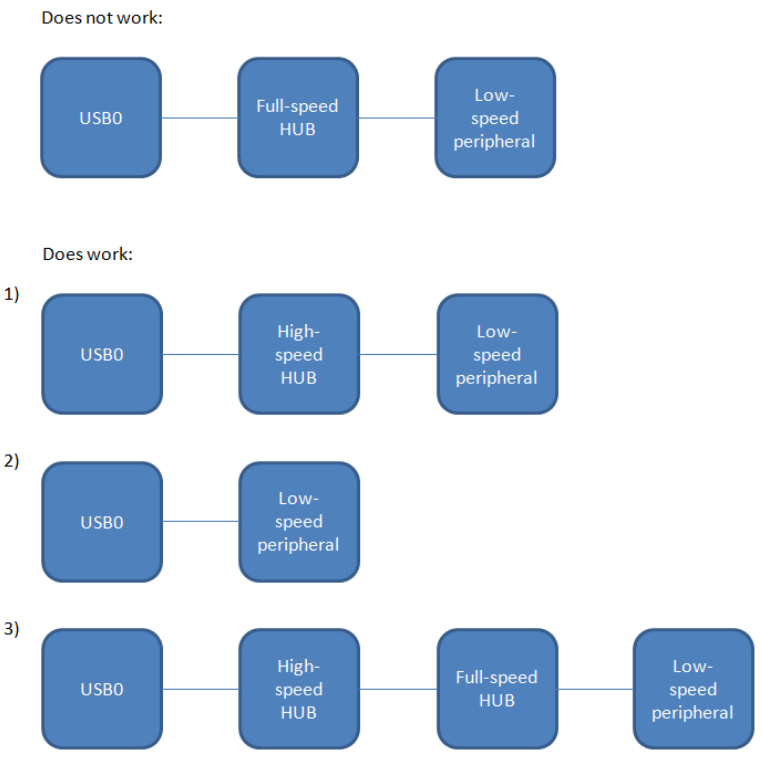

Fig 1. Suggested USB0 to low-speed peripheral connections

3.6 USB.2

Introduction:

The LPC18S5x flash-based devices contain an event handler for USB SOF detection from the host called the USB_SOF_Event. When it is enabled this event fires at the start of each USB frame, once per millisecond in full-speed mode or once per 125 microseconds in high-speed mode, and is synchronized to the USB bus.

Problem:

The USB_SOF_Event may fire earlier than expected and/or an additional (false) interrupt may be generated.

Work-around:

There is no work-around. The USB_SOF_Event cannot be used in full-speed and high-speed device mode in case the system needs an interrupt that is aligned with the incoming SOF tokens.

3.7 USBROM.1

Introduction:

The USB ROM drivers include a default endpoint 0 handler which acts on events generated by the USB controller as a result of traffic occurring over the control endpoint. The user has the option of overloading this default handler for the purpose of performing user specific processing of control endpoint traffic as required.

One of the actions the default endpoint 0 handler performs is to prepare the DMA engine for data transfer after the controller has sent out a NAK packet to the host controller. This is done in preparation for the arrival of the next OUT request received from the host.

Problem:

Due to a race condition there is the chance that a second NAK event will occur before the default endpoint0 handler has completed its preparation of the DMA engine for the first NAK event. This can cause certain fields in the DMA descriptors to be in an invalid state when the USB controller reads them, thereby causing a hang.

Work-around:

Override the default endpoint 0 handler to add checks for and prevents nested NAK event processing activity.

This is an example of how to do this:

```
// Endpoint 0 patch that prevents nested NAK event processing
static uint32_t g_ep0RxBusy = 0; /* flag indicating whether EP0 OUT/RX buffer is
busy. */
static USB_EP_HANDLER_T g_Ep0BaseHdlr; /* variable to store the pointer to base EP0
handler */

/*-------------------------------------------------------------------------
  EP0_patch :
 *-------------------------------------------------------------------------*/
ErrorCode_t EP0_patch(USBD_HANDLE_T hUsb, void* data, uint32_t event)
{

    switch (event) {
        case USB_EVT_OUT_NAK:
            if (g_ep0RxBusy) {
                /* we already queued the buffer so ignore this NAK event. */
                return LPC_OK;
            } else {
                /* Mark EP0_RX buffer as busy and allow base handler to queue the
     buffer. */
                g_ep0RxBusy = 1;
            }
            break;
        case USB_EVT_SETUP: /* reset the flag when new setup sequence starts */
        case USB_EVT_OUT:
            /* we received the packet so clear the flag. */
            g_ep0RxBusy = 0;
```

```
            break;
    }
    return g_Ep0BaseHdlr(hUsb, data, event);
}


// Install the endpoint 0 patch immediately after USB initialization via the
     hw->Init() call.

*-------------------------------------------------------------------------
  usbd_init: usb subsystem init routine
*-------------------------------------------------------------------------*/
ErrorCode_t usbd_init (void)
{
    USBD_API_INIT_PARAM_T usb_param;
    USB_CORE_DESCS_T desc;
    ErrorCode_t ret = LPC_OK;
    USB_CORE_CTRL_T* pCtrl;


…
    /* USB Initialization */
    ret = USBD_API->hw->Init(&g_AdcCtrl.hUsb, &desc, &usb_param);
    if (ret == LPC_OK) {

        /* register EP0 patch */
        pCtrl= (USB_CORE_CTRL_T*)g_AdcCtrl.hUsb; /* convert the handle to control
     structure */
        g_Ep0BaseHdlr = pCtrl->ep_event_hdlr[0]; /* retrieve the default EP0_OUT
     handler */
        pCtrl->ep_event_hdlr[0] = EP0_patch;     /* set our patch routine as EP0_OUT
     handler */


….'
  }
….'
  return LPC_OK;
}
```

3.8 USBROM.2

Introduction:

The USB ROM drivers configure and manage data structures used by the USB controller's DMA engine to move data between the controller's internal fifos and system memory. The configuration of these data structures are based on many parameters including the type of transfer, control, bulk, interrupt, or isochronous, that is to be performed. These data structures reside in system RAM on a 2 kB boundary and are pointed to by the ENDPOINTLISTADDR register.

Problem:

The USB ROM drivers incorrectly configures the Endpoint Capabilities/Characteristics field of the device Queue Head (dQH) structure for isochronous endpoints. Specifically, the MULT member is set to 0 and the ZLT member is set to 1. Also if the maximum size of isochronous packets are 1024 bytes the Max_packet_length member will be set to 0. For any other packet size this member is set correctly.

Work-around:

To use isochronous transfers with the USB ROM drivers the Endpoint Capabilities/Characteristics field must be correctly configured for that endpoint's device Queue Head structure. The USB ROM driver always sets this field (incorrectly) when the host sends a Set Interface control packet and then it calls the USB_Interface_Event callback routine, so the field must be set with the proper value in this callback routine.

This is the device Queue Head structure:

```
typedef volatile struct
{
  volatile uint32_t cap;
  volatile uint32_t curr_dTD;
  volatile uint32_t next_dTD;
  volatile uint32_t total_bytes;
  volatile uint32_t buffer0;
  volatile uint32_t buffer1;
  volatile uint32_t buffer2;
  volatile uint32_t buffer3;
  volatile uint32_t buffer4;
  volatile uint32_t reserved;
  volatile uint32_t setup[2];
  volatile uint32_t gap[4];
}  DQH_T;
```

This is an Interface Event callback routine:

```
ErrorCode_t USB_Interface_Event (USBD_HANDLE_T hUsb)
{
     USB_CORE_CTRL_T* pCtrl = (USB_CORE_CTRL_T*)hUsb;
     uint16_t wIndex = pCtrl->SetupPacket.wIndex.W; // Interface number
     uint16_t wValue = pCtrl->SetupPacket.wValue.W; // Alternate setting number

     if (wIndex == isochronous_interface_number && wValue == 1)
     {
```

```
            DQH_T* ep_QH = *(DQH_T**)0x40006158; // ENDPOINTLISTADDR register
            int QH_idx = ((endpoint_address & 0x0F) << 1) + 1;

            ep_QH[QH_idx].cap = ((packets_executed_per_transaction_descriptor << 30) |
      (maximum_packet_size << 16));
      }

  return LPC_OK;
}
```

The value of isochronous_interface_number should correspond to the interface number in the USB descriptor that holds the isochronous endpoint you wish to use.

The value of maximum_packet_size should correspond to the wMaxPacketSize member of the isochronous endpoint descriptor.

The value of endpoint_address should correspond to the bEndpointAddress member of the isochronous endpoint descriptor.

3.9 SD/MMC.1

Introduction:

The LPC18Sxx parts have the SD/MMC interface. After power up, the SD memory card is in the default speed mode, and by using the Switch Function command (CMD6), the Version 1.10 and higher SD memory cards can be placed in High-Speed mode. In response to the CMD6 command, the SD card returns a 512-bit block of data containing the available features and actual settings. The SDIO interface is setup for 4-bit data and therefore, the 512 bits are returned on the four data lines in 128 clocks followed by 16 clocks of CRC data.

Problem:

The CMD6 returned status block always gets a data CRC error although the status data is correct. The data CRC error prevents the switching of SD memory card from the default mode to High-Speed mode.

Work-around:

To capture the 512 bits of data and CRC data, the DMA buffer length and SD/MMC BYTCNT are increased to 72 and then the CRC is calculated in software. If the CRC is correct for all four data lines, the error is cleared.

3.10 RESET.1

Introduction:

The LPC18Sxx parts contain a Reset Generation Unit (RGU) that generates various resets; Core Reset (CORE_RST), Peripheral Reset (PERIPH_RST), Master Reset (MASTER_RST), and M3 Reset (M3_RST).

Problem:

On the LPC18Sxx, MASTER_RST and M3_RST are not functional.

Work-around:

There is no work-around. To reset the entire chip use the CORE_RST instead of using MASTER_RST or M3_RST.

3.11 RESET.2

Introduction:

The LPC18Sxx devices are initialized after a reset. If a reset occurs via nRESET pin when the part is in Deep-sleep or Power-down mode, the initialization state of the device may be erroneous and some functionality of the device may be lost.

Problem:

When the part is in deep-sleep or power-down mode and if an external reset occurs via nRESET pin being activated, as the part comes out of reset, the reset state of some functional blocks may be incorrect. This may result in loss of functionality of the device. The actual functionality lost may vary from part to part depending on the erroneous reset state of the functional blocks. The possible affected blocks are: Ethernet, LCD controller, CAN0, CAN1, USB0, USB1, AES, SRAM size at 0x2000 0000 may change to 16 kB, SRAM size at 0x2000 8000 may change to 0 kB, and SRAM size at 0x2000 C000 may change to 0 kB.

Work-around:

There are two possible work-arounds:

1. In the application software, before initializing peripherals, the code should assert a soft reset using the following steps:
   a. Read the value in power-down modes register (PD0_SLEEP0_MODE).
   b. If the value in the PD0_SLEEP0_MODE0 register represents deep-sleep mode or power-down mode, the user should check if a reset event occurred on the nRESET pin (bit ‘19’ in the Event Status register).
   c. If the reset event occurred, the software should set the PD0_SLEEP0_MODE register to deep power-down mode and assert a soft reset using the CORE_RST (bit ‘0’ in the RESET_CTRL0 register).

```
/* Check if wake up event happens in Deep Sleep or Power Down mode */
    if((LPC_PMC->PD0_SLEEP0_MODE == PMC_PWR_DEEP_SLEEP_MODE)
|| (LPC_PMC->PD0_SLEEP0_MODE == PMC_PWR_POWER_DOWN_MODE))
    {
        /* Check if the wake up event is due to nRESET pin in Event router */
        if(LPC_EVRT->STATUS & (1<<19))
        {
            /* Set power state in PMC */
            LPC_PMC->PD0_SLEEP0_MODE = PMC_PWR_DEEP_POWER_DOWN_MODE;
            /* Set CORE_RST in RGU */
            LPC_RGU->RESET_CTRL0 = (1<<0);
        }
    }
```

2. To initialize the device correctly, assert a second external reset signal to the nRESET pin after 20 μs from the first reset.

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